UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,729	03/29/2004	Tomoaki Toda	119312	9667

25944 7590 03/09/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
SAYADIAN, HRAYR A	

ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/810,729	TODA, TOMOAKI	
	Examiner	Art Unit	
	Hrayr A. Sayadian	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/29/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

CLAIM REJECTIONS - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,677,52 to Ogura [hereinafter "Ogura"].

With respect to claim 1: As to claim interpretation, the recitation "successively" in claims 1-15 is read broadly to include following each other but not necessarily without other layers in between (see claim 13 reciting a traveling layer between the earlier recited successive p-type base and active layers).

As to claim rejection, Ogura discloses a semiconductor laser (see for example Ogura column 3, lines 29-35) comprising a semiconductor layer group, wherein said semiconductor layer group is composed of an n-type emitter layer (see, for example, column 2, lines 3-4) a p-type base layer (column 2, lines 4-6), an active layer (column 2, lines 30-34), an n-type base layer (column 2, lines 6-7), and a p-type emitter layer (column 2, lines 7-8) which are successively formed on a given substrate. See also FIG. 1, as described in column 3, line 66 to column 4, line 31.

With respect to claims 2-7: The additional recitations in claims 2-7 are directed to intended manner of using the laser diode. The device disclosed in Ogura reads on claim 1, from which claims 2-7 depend, and it can be used in the intended manner recited in claims 2-7.

With respect to claims 8: The recitation defining the first semiconductor layer group functioning as a bipolar transistor verbally defines the layers forming one of the two bipolar transistors forming any thyristor. Such recitation fails to further structurally narrow claim 8 with respect to claim 1, from which claim 8 depends. The additional

recitation in claim 8 is directed to the intended manner of using the laser diode. The device disclosed in Ogura reads on the device of claim 1 and it can be used in the intended manner recited in claim 8.

With respect to claims 9: The recitation defining the second semiconductor layer group functioning as a bipolar transistor verbally defines the layers forming the other one of the two bipolar transistors forming any thyristor. Such recitation fails to further structurally narrow claim 9 with respect to claim 8, from which claim 9 depends. The additional recitation in claim 9 is directed to the intended manner of using the laser diode. The device disclosed in Ogura reads on the device of claim 8 and it can be used in the intended manner recited in claim 9.

With respect to claims 10: The additional recitation in claim 10 is directed to the intended manner of using the laser diode. The device disclosed in Ogura reads on claim 9, from which claim 10 depends, and it can be used in the intended manner recited in claim 10.

With respect to claim 11 and 12: See for example Ogura column 3, line 66 to column 4, line 39, describing FIGs. 1 and 2 and disclosing making the semiconductor layer group of III-V semiconductor compound (GaAs).

With respect to claims 13 –15: See for example Ogura column 3, lines 35-46, describing the make and function of layer 31 of FIG. 1. See also FIG. 2 showing InGaAs as partly making the layer 31.

With respect to claims 16 and 17: As to claim interpretation, the recitation "successively" in claims 16 and 22-24 is read broadly to include the layers following each other but not necessarily without other layers in between (see claim 13 reciting a traveling layer between the earlier recited successive p-type base and active layers).

As to claim rejection, Ogura discloses a method for oscillating a semiconductor layer group composed of an n-type emitter layer, a p-type base layer, an active layer, an n-type base layer and a p-type emitter layer which are successively formed on a given substrate, comprising a step of: applying a voltage to said active layer to generate a drift current therein (See for example FIG. 4, control light 61 through transistor 41, and control light 62 through transistor 40, as changing the affect of bias source 50 on the second/third

opposite conductivity layers; the application of reset light 62 on transistor 40 backward biases the second/third conductivity layers with the active region in between by raising the voltage of the n layer, to which the emitter of transistor 40 is connected, with respect to the p layer below it; this backward biasing generates a drift current, which passes through the active region and thus generates and oscillates light of a given wavelength; see column 5, lines 8-29, describing the embodiment of FIG.4) so that said active layer is excited by said drift current to generate and oscillate a light of a given wavelength.

With respect to claims 18 and 19: As to claim interpretation, the recitation "successively" in claims 18 and 19 is read broadly to include the layers following each other but not necessarily without other layers in between (see claim 13 reciting a traveling layer between the earlier recited successive p-type base and active layers).

As to claim rejection, Ogura discloses a method for oscillating a semiconductor laser comprising a semiconductor layer group composed of an n-type emitter layer, a p-type base layer, an active layer, an n-type base layer and a p-type emitter layer which are successively formed on a given substrate, comprising a step of: applying a voltage to said active layer to generate a diffusion current therein (see for example FIG. 4, the control light 61 on transistor 41 forward biases the second/third opposite conductivity layers with the active region in between; this forward biasing generates a diffusion current, which passes through the active region and thus generates and oscillates light of a given wavelength; see column 5, lines 8-29, describing the embodiment of FIG.4) so that said active layer is excited by said diffusion current to generate and oscillate a light of a given wavelength.

With respect to claim 20: As to claim interpretation, the recitation "successively" in claims 20 and 21 is read broadly to include the layers following each other but not necessarily without other layers in between (see claim 13 reciting a traveling layer between the earlier recited successive p-type base and active layers).

As to claim rejection, Ogura discloses a method for oscillating a semiconductor laser comprising a semiconductor layer group composed of an n-type emitter layer, a p-type base layer, an active layer, an n-type base layer and a p-type emitter layer which are

successively formed on a given substrate, comprising a step of: applying a voltage to said active layer to generate a diffusion current (see explanation describing rejection of claims 18 and 19) and a drift current therein (see explanation describing rejection of claims 16 and 17) so that said active layer is excited by said diffusion current and said drift current to generate and oscillate a light of a given wavelength.

With respect to claim 21: Ogura discloses a method for oscillating wherein two kinds of forward voltages are applied to a pn junction composed of said p-type base layer, said active layer and said n-type base layer (the application of a controlling pulse on transistor 41 inherently results in a rise-time for the applied forward voltage on the second/third opposite conductivity regions, with the active layer in between, either due to the rise-time of the applied optical pulse or due to the effective RC time of the circuit, or due to both; the rising of the applied voltage yields many kinds of forward as the voltage increases—which, when the voltage source 50 is higher than the inherent barrier potential, includes a forward voltages below the inherent barrier voltage at the beginning of the rising voltage and a forward voltage above the inherent barrier voltage when the risetime effect ends).

With respect to claims 22: Ogura discloses a method for oscillating wherein said n-type emitter layer, said p-type base layer, said active layer and said n-type base layer, which are successively formed, constitute a first semiconductor layer group functioning a bipolar transistor, and by driving said first semiconductor layer group, an amount of electrons to be injected into said active layer is controlled (see the explanation describing the rejection of claim 8).

With respect to claim 23: Ogura discloses a method for oscillating wherein said p-type base layer, said active layer, said n-type base layer and said p-type emitter layer, which are successively formed, constitute a second semiconductor layer group functioning a bipolar transistor, and by driving said second semiconductor layer group, an amount of holes to be injected into said active layer is controlled (see the explanation describing the rejection of claim 8).

With respect to claim 24: Ogura discloses a method for oscillating wherein said semiconductor layer group includes an electron traveling layer between said p-type base layer and said active layer, whereby a current oscillation due to Gunn effect of said semiconductor layer group achieves a high-speed modulation of light intensity due to a relaxation oscillation of said semiconductor laser so that an intensity of said light generated and oscillated can be modulated at high speed (Absent a step describing causing the Gunn effect specific to the disclosure by this application, Ogura discloses a structure reading on the semiconductor layer group of this application and therefore a current oscillation due to the Gunn effect can also be generated by the structure Ogura discloses, which current oscillation achieves ...).

ADDITIONAL PRIOR ART OF RECORD

3. U.S. Pat. Nos. 3,577,018; 3,585,520; 4,352,116; 3,757,174 and 4,065,729 to Wada, Yanai et al, Yariv et al., Shigermasa et al., and Gover et al., respectively, disclose Gunn effect structure along with semiconductor lasers (the first three references), a PNPN laser diode exhibiting a negative resistance characteristic (the fourth reference) and using monolithic PNPN injection lasers (the fifth reference).

CLOSURE

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hrayr A. Sayadian whose telephone number is (571) 272-7779. The examiner can normally be reached on Monday through Friday, 7:30 am to 4:00 pm, ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun O. Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HAS